

Curriculum Vitae

Yan Zhang

Computer Science Department,
University of California at Los Angeles
4651 Boelter Hall
Los Angeles, CA 90095-1596

Tel (lab): (310) 206-2279,
Cell: (310) 309-0720
Fax: (310) 825-2273
Email: zhangyan@cs.ucla.edu
URL: <http://cadlab.cs.ucla.edu/~zhangyan>

Education

University of California at Los Angeles, Los Angeles, CA

Ph.D in Computer Science, June 2006 (expected) Advisor: Prof. Jason Cong
Thesis: Multilevel Routing for Higher Degree of Circuit Integration

Tsinghua University, Beijing, China

M.S in Computer Science and Applications, June 2000 Advisor: Prof. Xianlong Hong,
Thesis: Algorithms for Bus Routing and Gridless Area Routing

Zhejiang University, Hangzhou, China

B.S in Computer Science and Engineering, June 1997

Research Interests

Highly scalable VLSI physical design algorithms, especially multilevel full-chip routing

Design tools for emerging IC manufacturing and integration technologies, such as 3D ICs, nano technologies, etc.

Thermal modeling and optimization, thermal aware design automation

Algorithmic design and applications

Discrete and continuous optimization

Professional Affiliations

ACM/IEEE student member

ACM Special Interest Group Design Automation

IEEE Women in Engineering

Related Publications

1. J. Cong, J. Wei, and **Y. Zhang****, "Thermal-Aware 3D IC Placement Via Transformation," submitted to *DAC* 2006.
2. J. Cong, A. Jagannathan, Y. Ma, G. Reinman, J. Wei, and **Y. Zhang**, "An Automated Design Flow for 3D Microarchitecture Evaluation," to appear in *ASPDAC* 2006.

3. J. Cong and **Y. Zhang****, "Thermal Via Planning for 3D ICs," *Proceedings of the 2005 IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, November, 2005.
4. J. Cong and **Y. Zhang****, "Thermal-Driven Multilevel Routing for 3-D ICs," *Proceedings of the Asia South Pacific Design Automation Conference*, January 2005.
5. J. Cong, J. Fang, M. Xie, and **Y. Zhang****, "MARS - A Multilevel Full-Chip Gridless Routing System," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 24, No. 3, pp. 382-394, March 2005.
6. J. Cong, J. Wei, and **Y. Zhang****, "A Thermal-Driven Floorplanning Algorithm for 3D ICs," *Proceedings of the 2004 IEEE/ACM International Conference on Computer-Aided Design*, November 2004.
7. J. Cong, M. Xie, and **Y. Zhang****, "Chapter 5 Multilevel VLSI Routing," *Multilevel Optimization in VLSICAD*, Kluwer Academic Publishers, 2003.
8. J. Cong, M. Xie, and **Y. Zhang****, "An Enhanced Multilevel Routing System," *Proceedings of the 2002 IEEE/ACM International Conference on Computer-Aided Design*, November 2002.
9. J. Cong, J. Fang, and **Y. Zhang****, "A Multilevel Approach to Full-Chip Gridless Routing," *Proceedings of the 2001 IEEE/ACM International Conference on Computer Aided Design*, San Jose, California, pp. 396-403, November 2001. (**nominated for the best paper award**)
10. Yiqian Zhang, Y. Cai, X. Hong, **Y. Zhang**, and X. Min, "A Gridless Router Based on Hierarchical PB Corner Stitching Structure," *The Chinese Journal of Semiconductors*, vol. 24, 2003. (in Chinese)
11. **Y. Zhang****, B. Wang, Y. Cai, and X. Hong, "Area Routing Oriented Hierarchical Corner Stitching with Partial Bin," *The Chinese Journal of Computers*, vol. 7, 2000. (in Chinese)
12. Yiqian Zhang, **Yan Zhang**, Y. Cai and X. Hong, "An algorithm for bus routing based on line-probe," *Microelectronics*, S0:13, 2000. (in Chinese)
13. **Y. Zhang****, B. Wang, Y. Cai, and X. Hong, "Area Routing Oriented Hierarchical Corner Stitching with Partial Bin," *Proceedings of the Asia South Pacific Design Automation Conference*, January 2000.

Note*: All publications co-authored with members in Professor Jason Cong's research group list co-authors in alphabetical order.

** indicates that I am the principle author for this paper.

Research Experience

Research Assistant, VLSI CAD Lab, UCLA

- Designed and developed the **first** published multilevel routing system, MARS, under the support of GSRC and NSF
- Provided a **key** role to the DARPA-sponsored project, "Advanced Physical Design Tools for 3-Dimensional Integrated Circuits" (subcontract from CFDRC), including proposal writing, project planning, reporting, and coordination.
 - **Led** the development of the whole 3D thermal-aware physical design flow
 - Designed and led the development of the **first** published thermal-aware 3D floorplanner
 - Designed and developed a novel thermal-aware 3D placement via transformation
 - Designed and developed the **first** published thermal-aware 3D router
- Designed and developed a novel 3D thermal via planner with alternating direction planning, where vertical via planning is solved **optimally**

Sep. 2000 -
Present

Internship at Motorola at Austin, TX,

- Designed and developed a novel fixed-length clock routing algorithm with snaking, shielding, bus routing and grouping. The router has been incorporated into the in-

Summer 2003

house design tool and used for microprocessor designs.

Research Assistant, VLSI CAD Lab, Tsinghua University,

- Took a key role in the gridless detailed routing project, proposed and developed a fast hierarchical layout database and led the development of the routing engine Sep. 1997 – Jun. 2000
- Designed and developed a bus routing algorithm based on line-search and bend type determination

Undergraduate Researcher, Institute of Artificial Intelligence, Zhejiang University

Sep. 1995 – Jun. 1997

- Developed algorithms for shot detection and tracking of the moving objects.

Teaching and Advising Experience

Teaching Assistant

- Undergraduate Course, “CS152A, Digital Design Laboratory”, University of California at Los Angeles. Winter 2003.

Delivered lectures on using Altera MAX+PLUSII and FPGAs for digital circuit design projects, the purpose, the design flow and the critical steps of each lab project. Designed exercise questions for pre-lab reports and lab reports. Supervised and guided students in doing their projects. Contributing in designing the final exam. Graded pre-lab reports, lab reports, and final exams.

Advising

- I have supervised and directed the following undergraduate/graduate students in their research projects:

Guojie Luo – graduate student at UCLA, Sep. 2005 – present.

Project: “Thermal-aware placement algorithms”

Thomas Carriero – undergraduate student at Harvard, Summer 2005

Project, “parallel design rule checking algorithms on multi-core machines”

Jie Wei – graduate student at UCLA, Sep. 2003-Nov. 2004

Project, “Thermal-aware 3D Floorplanning”

Yiqian Zhang – graduate student at Tsinghua University, Jan. 2000 – Jun. 2000

Project: “ a line-probe based bus routing”

Contribution in Grants and Proposals

“Closing the Gap in VLSI Physical Design”

Principal Investigator : Jason Cong, Co-Principal Investigator: Tony Chan

National Science Foundation

Fund: \$200000 Sep. 2004 - Aug. 2006

Contributed key sections to the research proposal

“Advanced Physical Design Tools for 3-Dimensional Integrated Circuits”

Principal Investigator: Marek Turowski

Jun.2002 - Nov.2005

Contributed key sections to the proposals, whitepapers, monthly reports and final reports

Academic Service

Technical program committee member: ASPDAC2004

Reviewer: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems(TCAD), IEEE Transactions on Very Large Scale Integration (VLSI) Systems, ACM Transactions on Design Automation of Electronic Systems (TODAES), Integration, the VLSI Journal, Proceedings of IEEE, International Conference on Computer Aided Design (ICCAD), International Symposium on Physical Design (ISPD), International Symposium on Field-Programmable Gate Arrays (FPGA), Asia and South Pacific Design Automation Conference (ASPDAC), International Symposium on Low Power Electronics and Design (ISLPED), IEEE International Symposium on Circuits and Systems (ISCAS), IEEE International Conference on Computer Design (ICCD), Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI), GLSVLSI

Honors

1998-1999 Excellent Student Scholarship, Tsinghua University

Graduation with Honors, 1997, Zhejiang University

June 1997, Excellent Diploma Thesis

1994 - 1996 Excellent Student Scholarship, Zhejiang University

Graduation with Honors, 1995, Mixed Class (two year elite program for top 3% out of 3000 students), Zhejiang University

Personal Information

Place of Birth:	Hangzhou, China
Citizenship:	China
Visa Status:	F1
Gender:	Female

References

Prof. Jason Cong

UCLA Computer Science Department,
4731J, Boelter Hall,
Los Angeles, CA 90095.
Phone: (310) 206-2775
Fax: (310) 825-2273
E-mail: cong@cs.ucla.edu

Dr. Marek Turowski

CFD Research Corp.
215 Wynn Drive, 5th Floor
Huntsville, AL 35805
Tel: (256) 726-4889
Fax : (256) 726-4806
Email: mt@cfdr.com

Prof. Sachin Sapatnekar

Department of Electrical and Computer Engineering
University of Minnesota
200 Union Street SE,
Minneapolis, MN 55455.
Tel: (612) 625-0025,
Fax: (612) 625-4583
Email: sachin@ece.umn.edu

Prof. Tony Chan

UCLA Dept of Mathematics,
Los Angeles, CA 90095-1555
Tel: (310) 825-4831
Fax: (310) 206-6673
Email: chan@math.ucla.edu

Prof. Majid Sarrafzadeh

UCLA Computer Science Department
3532C Boelter Hall
Los Angeles, CA 90095
Phone: 310-794-4303
Fax: (310) 825-2273
Email: majid@cs.ucla.edu